REMARKS

Claims **1-20** are pending in the present application after entry of the present amendment. Claims 4, 5, 9, 11 and 12 were rejected under 35 U.S.C. 112. Claims 1-12 were rejected under 35 U.S.C. 102(b). Claims 13-20 were rejected under 35 U.S.C. 103(a).

Applicant requests the favorable reconsideration of the claims and withdrawal of the pending rejections and objections, in view of the present amendment and in light of the following discussion.

Claim Rejections under 35 USC 112

Claims 4, 5, 9, 11 and 12 were rejected under 35 U.S.C. 112 as being indefinite. These claims have been amended to remove the indefiniteness; hence these rejections are requested to be withdrawn.

Claim Rejections under 35 USC 102: Claims 1 - 9

Claims 1-9 were rejected under 35 U.S.C. 102(b) as being anticipated by Ooishi (JP 2000244287, references herein refer to the U.S. counterpart, U.S. Patent No. 6,433,586 B2).

Cited Prior Art

Ooishi discloses a flip-flop having a master latch circuit 22 connected to a slave latch circuit 24 (see Fig. 9). When TG1 is high, inputs D and /D are allowed to pass through circuit 21 to master latch circuit 22. Transistor PQ5 is non-conductive and the transmission gate CQ1 is conductive. Little current flows, because circuit 22 is cut off from the VCC power supply. The output nodes OD1 and OD2 are equalized by the transmission gate CQ1 and are both reduced via either transistor NT1 or NT2 in order to reduce the output voltage level. (col. 16, lines 47-64). In the master latch circuit 22, when TG1 is low, transistor PQ5 is conductive and the transmission gate CQ1 is non-conductive, and a latch operation occurs using cross coupled transistors PT1 and PT2 (col. 17,

lines 1-16). When TG1 is low, TG2 is high and the outputs of the master latch circuit (D3 and /D3) are allowed via circuit 23 to go to the slave latch circuit 24. The transistor NT3 is conductive and the VCC power supply transistor PQ6 is nonconductive. Hence the voltages of the output nodes D5 and /D5 are equalized, and there is little current flowing in circuit 24. When clock TG2 goes low, transistor NT3 is non-conductive, power supply transistor PQ6 is conductive, and a latch operation occurs (col. 17, lines 17 - 38).

Prior Art Distinguished

Claim 1 recites a flip-flop having, among other features, a cross coupled circuit having a cross coupled transistor directly connected to a power supply voltage, wherein a gate of the cross coupled transistor is connected to the second output terminal. Oiishi neither discloses nor suggests such a feature. In Oiishi the master latch 22 and the slave latch 24 are conditionally connected to the power supply VCCC or PS1 via PMOS transistors PQ5 and PQ6, respectively. These transistors are turned on and off depending on the state of clock signals TG1 or TG2. Oiishi does not disclose or teach a cross-coupled transistor directly connected to a power supply voltage. Hence for at least this reason, Claim 1 should be allowable.

Claims 2 to 9 being dependent on Claim 1 should be allowable for at least the same reasons Claim 1 is allowable.

Claim Rejections under 35 USC 102: Claims 10 - 12

Claims 10 -12 were rejected under 35 U.S.C. 102(b) as being anticipated by Rollins et al. (U.S. Patent No. 5,036,217).

Cited Prior Art

Rollins discloses a master-slave flip-flop circuit as shown in Fig. 1B. When the clock is high the master portion 201 of flip-flop 200 is enabled (the slave portion 217 is disabled) and an input D is latched into the circuit via cross-

coupled transistors 202 and 204. When the clock signal goes low, the master portion 201 is disabled via transistor 210 and the slave portion 217 is enabled via transistor 212. The slave portion 217 then transfers the input D to the output Q . (col. 3, lines 22 - 63). Fig. 3B operates similar to Fig. 1B, except logic NAND and OR functions have been added (col. 4, lines 44 - 47).

Prior Art Distinguished

Claim 10 recites a flip-flop having, among other features, a differential input stage having a first transistor that has a first control terminal connected to the first input terminal and a current handling terminal directly connected to VSS. Rollins neither suggest nor discloses this feature. In Rollins all current handling terminals of transistors in input stage 601 are connected to ground via transistor 618. Transistor 618 is turned on and off by the clock signal in order to enable or disable the input stage. Rollins does not teach nor disclose an input stage transistor that has a control terminal connected to the first input terminal and a current handling terminal directly connected to ground. Thus for at least this reason claim 10 should be allowable.

Claims 11 and 12 being dependent on claim 10 should be allowable for at least the same reasons claim 10 is allowable.

Rejections under 35 U.S.C. 103: Claims 13 - 16

Claims 13 - 16 were rejected under 35 U.S.C. 103 as being unpatentable over Rollins in view of Choe (U.S. Patent No. 6,373,292).

Cited Prior Art

For Rollins see above.

Choe discloses a differential circuit for performing logic functions having precharge and evaluate phases. The precharge phase is when the clock signal is low and the evaluate phase is when the clock signal is high (col. 2 lines 25 to 31). Fig. 2

shows cross-coupled transistors 42 and 44 whose gates are coupled together low via transistor 56, when the clock signal is. During precharge phase gates 54 and 56 are set at a potential of about Vdd/2, hence partially turning on transistors 46 and 48. As transistor 52 is off, no current flows through transistors 46 and 48 and outputs 58 and 60 become about Vdd/2. When the clock goes high, transistor 52 turns on, and transistor 56 turns off. If the input is high then node 58 goes from Vdd/2 to 0 volts rather than Vdd to 0 volts.

Prior Art Distinguished

First, claims 13 - 16 being dependent on claim 10 should be allowable for at least the same reasons claim 10 is allowable. Second Choe cannot be combined with Rollins. Choe assumes that the inputs IN and /IN can be set at Vdd/2, when the clock is low, i.e., during precharge. Transistor 56 allows the outputs OUT and /OUT to also be Vdd/2. For arguments sake, assume that a transistor, like transistor 56, connected the outputs (631 and 633) of the first stage 601. The voltage levels of inputs Q1, Q1', MOD and MOD' of Fig. 3B in Rollins cannot be set like the inputs in Choe, because, as can be seen from Fig. 3B, Q1 and MOD are connected in series and Q1' and MOD' are connected in parallel. Thus for at least the above reasons claims 13 -16 should be allowable.

Rejections under 35 U.S.C. 103: Claims 17 - 20

Claims 17 - 20 were rejected under 35 U.S.C. 103 as being unpatentable over Figs. 1 and 2 of the application in view of Oiishi.

Claim 17 recites a counter having, among other features, a first flip-flop having: a differential output stage having differential first and second input terminals and complementary first and second output terminals; and a cross coupled circuit having a cross coupled transistor directly connected to a power

supply voltage, wherein a gate of the cross coupled transistor is connected to the second output terminal.

Oiishi's differential output stage has in circuit 24 a power supply transistor PQ6 which connects or disconnects a power supply voltage PS1. . Oiishi does not disclose or teach a cross-coupled transistor directly connected to a power supply voltage. Hence replacing each of the flip-flops in Fig. 1 with the flip-flop of Fig. 9 of Oiishi does not meet all the limitations of claim 17. Thus the rejection should be withdrawn and the claim allowed.

Claims 18 - 20 being dependent on claim 17 should be allowable for at least the same reasons claim 17 is allowable.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) is/are captioned **"Version with markings to show changes made."**

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D. C. 20231, on January 4, 2003.

Pat Slaback
Name

Signature

VERSIONS WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS

1. (Amended) A flip-flop comprising:

a. a differential output stage having differential first and second input terminals and complementary first and second output terminals; **[and]**

c. a transistor having a first current-handling terminal connected to the first output terminal, a second current-handling terminal connected to the second output terminal, and a control terminal**[.]**; and

c. a cross coupled circuit having a cross coupled transistor directly connected to a power supply voltage, wherein a gate of the cross coupled transistor is connected to the second output terminal.

4. (Amended) The flip-flop of claim **[1]** 3, further comprising a first clock terminal connected to the first-mentioned control terminal and a second clock terminal connected to the second control terminal.

9. (Amended) The flip-flop of claim 8, wherein the **[first and second clock]** control and second control terminals are adapted to receive complementary clock signals.

10. (Amended) A flip-flop comprising a differential input stage having differential first and second input terminals, differential third and fourth input terminals, a first transistor, and complementary first and second output terminals, wherein the first transistor has a first control terminal connected to the first input terminal and a current handling terminal directly connected to VSS.

11. (Amended) The flip-flop of claim 10, wherein the input stage further comprises a first leg including the first transistor and a second transistor**[s]** connected in parallel, the **[first]** second transistor having **[a first control terminal connected to the first input terminal and]** a second control terminal connected to the third input terminal.

17. (Amended) A counter circuit comprising:

a. a first flip-flop having:

i. a differential output stage having differential first and second input terminals and complementary first and second output terminals; and

ii. a first transistor having a first current-handling terminal connected to the first output terminal, a second current-handling terminal connected to the second output terminal, and a first control terminal; and

iii. a cross coupled circuit having a cross coupled transistor directly connected to a power supply voltage, wherein a gate of the cross coupled transistor is connected to the second output terminal; and

b. a second flip-flop having:

i. a differential input stage having differential third and fourth input terminals connected to the respective first and second output terminals of the first flip-flop, a second transistor, and complementary third and fourth output terminals, the second transistor having a gate connected to the third input terminal and a current handling terminal directly connected to VSS; and

ii. a third **[second]** transistor having a third current-handling terminal connected to the third output terminal, a fourth current-handling

terminal connected to the fourth output terminal, and a second control terminal.